METHOD AND CIRCUITRY FOR PRESERVING A LOGIC STATE

Abstract of the Disclosure

In response to a first transition of a clock signal, an information signal having a logic state is received. In response to a second transition of the clock signal, first circuitry latches a logic state of a first signal that indicates the information signal's logic state. In response to a third transition of the clock signal, second circuitry latches a logic state of a second signal that indicates the first signal's logic state. During a first mode of operation, power is supplied to the first and second circuitry. During a second mode of operation, power is reduced to the first circuitry, while power is supplied to the second circuitry, so that the first signal's logic state is lost, while the second signal's logic state is preserved.